MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

2015/2016 SESSION

EEN 7066 - ADVANCED COMPUTER ARCHITECTURE

(MEng MicroE)

05 JUNE 2016
2:30 P.M – 5:30 P.M
(3 Hours)

INSTRUCTION TO STUDENT

1. This Question paper consists of 5 pages including cover page with 4 Questions only.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the answer Booklet provided.

Question 1

a) What is the significance of Amdahl's Law? Use an example to illustrate your explanation.

[5 marks]

b) Evaluate the two alternative machines for a conditional branch instruction, as follows:

- Machine A: A condition code is set by a compare instruction and followed by a branch that tests the condition code.
- Machine B: A compare instruction is included implicitly in the branch statement itself.

On both machines, the conditional branch instruction takes 2 cycles, and all other instructions take 1 clock cycle. On machine A, 20% of all instructions executed are conditional branches; since every branch needs a compare instruction, it follows that another 20% of the instructions are compares. Because machine A does not have the compare included in the branch, its clock cycle time is 25% faster than machine B's. Evaluate the performance of both machines in terms of execution time to determine which machine is faster.

[8 marks]

c) A 400-MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle counts (Table Q1):

Instruction types	Clock cycle	Instruction count
Data Transfer	2	14,000
Control transfer	2	16,000
Integer arithmetic	1	50,000
Floating point arithmetic	2	20,000

Table Q1

By using this benchmark program, determine the following:

i. Average clock cycles Per Instruction (CPI) [4 marks]

ii. Effective computer performance in terms of Million Instructions Per Second (MIPS) [4 marks]

iii. Execution time (in milliseconds) [4 marks]

Continued...

Question 2

a) Figure Q2 is the block diagram for a single cycle DLX datapath. Briefly discuss the Instruction Fetch (IF), Instruction Decode (ID) and Write Back (WB) phases with the aid of Figure Q2.

[15 marks]

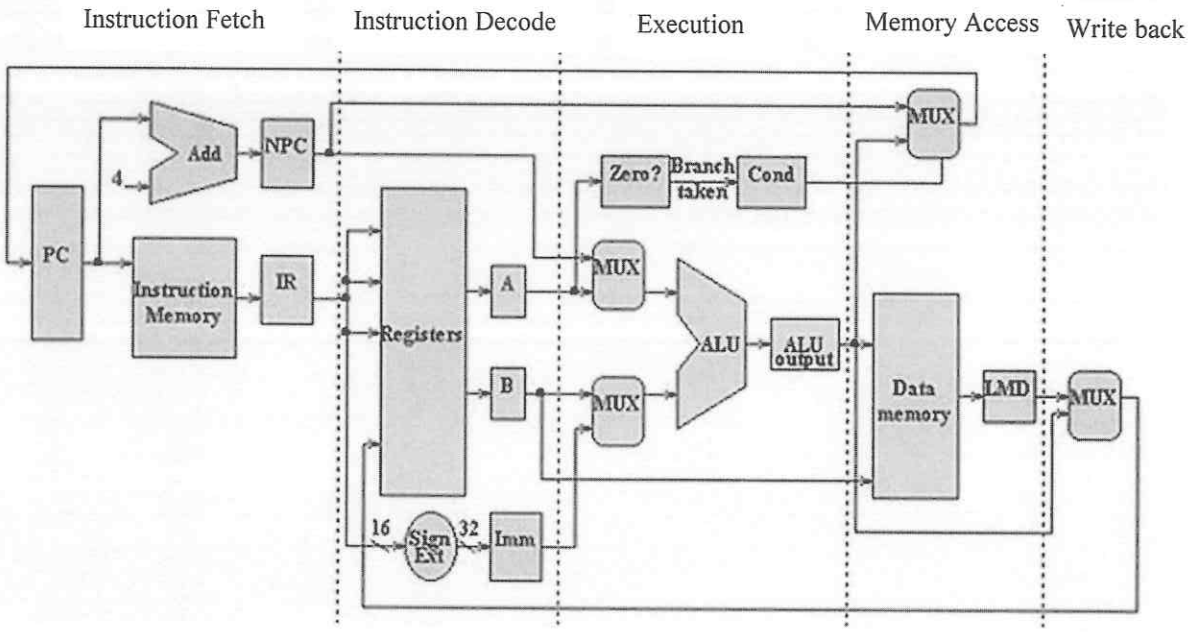

Figure Q2

b) Consider executing the following code segment on a five stages DLX pipelined datapath:

LW \$5, 200(\$7)

LW \$6, 170(\$8)

ADD \$4, \$5, \$6

SW 100(\$2), \$4

i. With the aid of diagrams, explain how the code segment will be executed (incorporating any stall or forwarding) so as to resolve any identified hazards.

[6 marks]

ii. How many **cycles** will it take to execute this code? [2 marks]

iii. What is the instruction latency on this pipelined machine with 5 execution stages of length 20ns, 30ns, 40ns, 15ns and 45ns? [2 marks]

Continued...

Question 3

a) Discuss the reason why there is a need for having a memory hierarchy in any computer system.

[5 marks]

b) Explain the concepts of cache memory. [4 marks]

c) Consider the C code (shown in Figure Q3c) for doing matrix operations, where it is assumed that all matrix elements within the same row are stored in contiguous locations. Answer the following question based on the code given.

```
for (I=0; I<1000; I++)
        for (J=0; J<100; J++)
                x[J][I]=y[J][I]+x[I][J];
```

Figure Q3c

i. Temporal locality is exploited when which variables are accessed? Justify your answer.

[5 marks]

ii. Spatial locality is exploited when which variables are accessed? Justify your answer.

[5 marks]

d) Figure Q3d shows two alternative ways of the parity calculation for RAID 4. Given that the data and parity blocks have values as follows:

New D0 = 6AED, Old D0 = 8F03, D1 = CEDF, D2 = 9B27, D3 = 63DB, P = FEFF

Show how to calculate the new RAID 4 parity value P*. [6 marks]

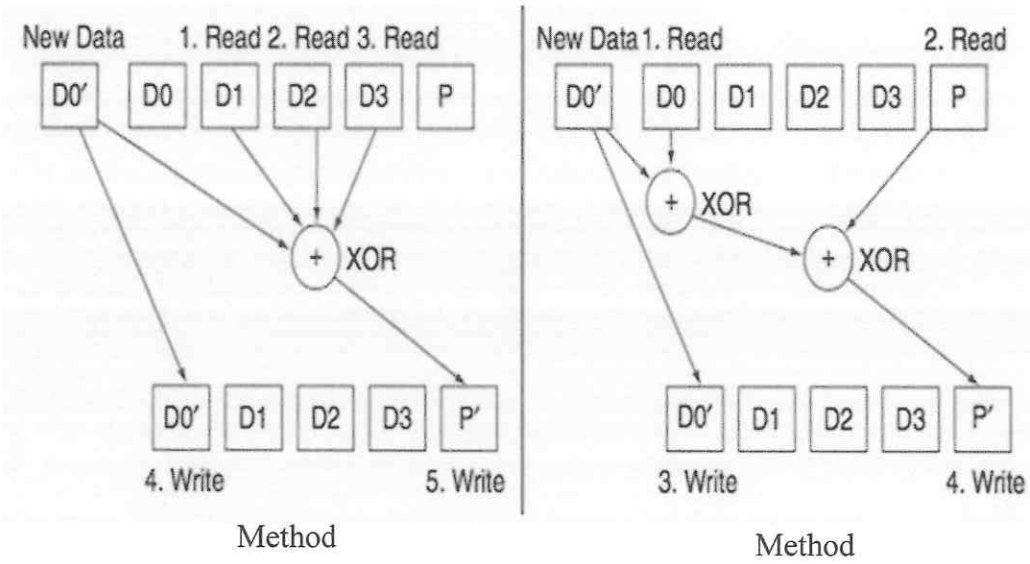

Figure Q3d : RAID 4 Parity example [Patterson & Hennessy 2012]

Question 4

a) Discuss the main potential bottlenecks that may be encountered when using a graphics processing unit (GPU) to perform calculations on data-intensive operations.

[6 marks]

b) Contrast between the following two settings:

i. Conventional: There are 8 computers, each with 8GB of main memory, out of which 5GB has to be taken up by the OS.

ii. Clustered computing: The 8 computers form a cluster, with access to a shared memory of 64GB within which the cluster OS occupies 5GB.

Calculate the ratio of available memory between the above two settings and discuss how much more space would users have in each setting. [6 marks]

c) Given that there are 1000 processors tasked to jointly compute the sum of 1,000,000 integers x1, x2, ..., x1000000, each performing its allocated task in parallel. Discuss how this task can be distributed to the processors and how the parallel computations can be aggregated towards obtaining the final sum.

[13 marks]

End of paper.